Claims

1. A semiconductor device having a source electrode, a drain electrode, a gate electrode disposed between the source electrode and the drain electrode, and a channel layer composed of a semiconductor which serves as a current path between the source electrode and the drain electrode, characterized by comprising:

a first barrier layer composed of a semiconductor having a p-type conductive region doped with a p-type impurity of high concentration under the gate,

a second barrier layer disposed on an opposite side of said first barrier layer while placing said channel layer in between and is composed of a semiconductor having an electron affinity smaller than that of said channel layer, and

a third barrier layer disposed between said first barrier layer and said channel layer and is composed of a semiconductor having an electron affinity smaller than that of said channel layer, wherein a relation below:

$$\chi_1 - \chi_3 \leq 0.5*(Eg_3 - Eg_1) \quad \ldots(1)$$

is satisfied, where χ_1 is electron affinity of said first barrier layer, Eg_1 is a band gap thereof, χ_3 is electron affinity of said third barrier layer, and Eg_3 is a band gap thereof.

2. The semiconductor device as claimed in Claim 1, characterized in that the semiconductor composing said third barrier layer is composed of a III-V compound semiconductor containing at least any one of Ga, Al and In as a Group III element, and containing at least either

one of As and P as a Group V element.

3. The semiconductor device as claimed in Claim 1, characterized in that the semiconductor composing said third barrier layer is InGaP or AlGaInP or InGaAsP.

4. The semiconductor device as claimed in Claim 1, characterized in that the semiconductor composing said third barrier layer is AlGaAs or AlGaAsP or AlGaInAs, having an Al composition ratio of 50% or more.

5. The semiconductor device as claimed in Claim 1, characterized in that a thickness of said third barrier layer is 20 nm or less.

6. The semiconductor device as claimed in Claim 1, characterized in that the semiconductor composing said first barrier layer is AlGaAs or GaAs or InGaP.

7. The semiconductor device as claimed in Claim 1, characterized by having a fourth barrier layer composed of a semiconductor having an electron affinity smaller than that of said channel layer and disposed between said third barrier layer and said channel layer.

8. The semiconductor device as claimed in Claim 7, characterized in that the semiconductor composing said fourth barrier layer is AlGaAs or GaAs.

9. The semiconductor device as claimed in Claim 7, characterized in that a sum of thicknesses of said third

barrier layer and said fourth barrier layer is 20 nm or less.

10. The semiconductor device as claimed in Claim 1, characterized by having a fifth barrier layer composed of a semiconductor having a band gap smaller than that of the first barrier layer and having a p-type conductive region doped with a p-type impurity of a high concentration, disposed between said first barrier layer and said gate electrode.

11. The semiconductor device as claimed in Claim 10, characterized in that the semiconductor composing said fifth barrier layer is GaAs.

12. The semiconductor device as claimed in Claim 1, characterized in that the p-type impurity doped to said first barrier layer is Zn.

13. The semiconductor device as claimed in Claim 1, characterized by having a sixth barrier layer composed of a semiconductor in which a Zn diffusion rate is slower than in the first barrier layer, disposed between said first barrier layer and said third barrier layer.

14. The semiconductor device as claimed in Claim 13, characterized in that the semiconductor composing said sixth barrier layer is GaAs or AlGaAs.

15. The semiconductor device as claimed in Claim 13, characterized in that a sum of thicknesses of said third

barrier layer and said sixth barrier layer is 25nm or less.

16. The semiconductor device as claimed in Claim 1, characterized in that, in a semiconductor layer on a gate electrode side in contact with said third barrier layer, a semiconductor layer which contains only one-tenth or less impurity as compared with a maximum impurity concentration of the p-type impurity contained in said first barrier layer exists in a thickness of 5 nm or more.

17. The semiconductor device as claimed in Claim 1, characterized in that at least any one layer of said first barrier layer, third barrier layer, fourth barrier layer and sixth barrier layer is doped with n-type impurity of high concentration.

18. The semiconductor device as claimed in Claim 1, characterized in that the semiconductor composing said channel layer is InGaAs or GaAs.